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DDR2 SPD INTERPRETATION OF TEMPERATURE RANGE AND (SELF-) REFRESH OPERATION

Introduction

The JEDEC standard DDR2 SDRAM must satisfy the requirement of 85C tCASE(max) operation at all times (Byte 47, bits 4:7 = 0000). There is an optional, higher tCASE operation allowed, up to 95C (Byte 47, bits 4:7 = 1010). If the optional higher tCASE limit is supported, there are two options that may or may not be supported to enhance the higher tCASE limit. These two options are vendor determined: (1) Double refresh required, (2) High Temp SR supported. If the base DRAM, i.e. tCASE(max) of 85C is specified, the two optional features are not required (but must be set to a default zero value.)

If, on the other hand, the optional tCASE(max) of 95C is supported, then the other two options must be specified as determined by the particular SDRAM supplier being used. JEDEC specifies that if a tCASE of 95C is used, then the refresh to the DRAM must be doubled (Byte 49, bit 1 = 1); however, a DRAM vendor may allow the normal refresh rate to be used (Byte 49, bit 1 = 0). Also, a particular SDRAM may support the higher tCASE option during self refresh (Byte 49, bit 0 = 1) while other SDRAMs will not (Byte 49, bit 0 = 0).

DDR2 SPD INTERPRETATION OF TEMPERATURE RANGE AND (SELF-) REFRESH OPERATION

(From JEDEC Board Ballot, JCB-05-117, formulated under the cognizance of the JC-42.3 Subcommittee on RAM Memories.)

1 Scope

The purpose of this document is to explain the meaning of SPD setting (JESD21 SPD section) for DDR2 SDRAM (JESD79-2) in normal and extended temperature operationy67.

2 DRAM Type & Description

Table 1 — DRAM Type & Descriptions

Type	Description
T1	<p>< 85 °C DRAM ></p> <p>Non-Self-Refresh operations supported up to Tcasemax = 85 °C with tREFI = 7.8 us.</p> <p>Self-Refresh Entry allowed at temperature up to Tcasemax = 85 °C.</p>
T2	<p>< 95 °C DRAM without the optional “High Temp Self-Refresh Rate Enable” feature ></p> <p>Non-Self-Refresh operations supported up to Tcasemax = 95 °C.</p> <p>Need tREFI adjustments to maintain refresh specifications. (tREFI = 7.8 us below 85 °C & tREFI = 3.9 us above 85 °C.)</p> <p>Self-Refresh Entry allowed at temperature up to Tcasemax = 85 °C.</p> <p>Requires ‘cool down’ before entering self-refresh mode.</p>
T3	<p>< 95 °C DRAM with the optional “High Temp Self-Refresh Rate Enable” feature ></p> <p>Non-Self-Refresh operations supported up to Tcasemax = 95 °C.</p> <p>Need tREFI adjustments to maintain refresh specifications. (tREFI = 7.8 us below 85 °C & tREFI = 3.9 us above 85 °C.)</p> <p>Self-Refresh Entry allowed at temperature up to Tcasemax = 95 °C.</p> <p>If entering SR at temperature above 85 °C, EMRS(2)[A7] must be programmed to 1 prior to SR Entry.</p> <p>Most likely, EMRS(2)[A7] information is used by the DRAM to set different internal Self-Refresh rates.</p> <p>EMRS(2)[A7] = 0: Recommended to be used for Self-Refresh Entry temperature of 0 °C to 85 °C.</p> <p>EMRS(2)[A7] = 1: May be used for Self-Refresh Entry temperature of 0 °C to 85 °C. Must be used for Self-Refresh Entry temperature of 85 °C to 95 °C.</p>

3 SPD Code vs. DRAM Type

Table 2 — SPD Code vs. DRAM Type

SPD Information			DRAM Type
Byte 47:	Byte 49:		
Δ Tcasemax: SPD code [bits 4:7] (Tcasemax)	Double Refresh required [Bit 1]	“High Temp SR” support [Bit 0]	
0 °C: 0000xxxx (85 °C)	0	0	Type T1: 85 °C DRAM
10 °C: 0101xxxx (95 °C)	1	0	Type T2: 95 °C DRAM without the “HT SR” Feature
	1	1	Type T3: 95 °C DRAM with the “HT SR” Feature

4 System Control Recommendation

Table 3 — System Control Recommendation

DRAM Type [Temp, SPD]	DRAM Control
T1 [85, 00]	<p>Recommended control.</p> <p>Ignore the information in Byte 49, Bit 1. Use fixed tREFI = 7.8 us. Program EMRS(2)[A7] = 0 and don't touch it. Never operate this DRAM above 85 °C.</p>
T2 [95, 10]	<p>Recommended control.</p> <p>Use adjustable tREFI; tREFI = 7.8 us below 85 °C & tREFI = 3.9 us above 85 °C. Program EMRS(2)[A7] to 0 and don't touch it. Always wait for the DRAM to 'cool down' below 85 °C before entering Self-Refresh.</p> <p>Options for simpler control.</p> <p>Use fixed tREFI = 3.9 us for the full temperature range of 0 °C to 95 °C. or Never put DRAM into Self-Refresh mode.</p>
T3 [95, 11]	<p>Recommended control.</p> <p>Use adjustable tREFI; tREFI = 7.8 us below 85 °C & tREFI = 3.9 us above 85 °C. Program EMRS(2)[A7] properly to 0 or 1 depending on the Self-Refresh Entry temp. If SR mode is entered above 85 °C, wake up the DRAM once temp drops below 85 °C, re-program the EMRS(2)[A7] to 0, then put it into Self-Refresh mode again.</p> <p>Options for simpler control.</p> <p>Use fixed tREFI = 3.9 us for the full temperature range of 0 °C to 95 °C. or Set EMRS(2)[A7] to 1 and never update it. or Don't perform the wake up sequence even if the temperature drops below 85 °C.</p>



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